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328356(28)

B. E. (Third Semester) Examination, April-May 2021

(New Scheme)

(Et&T Branch)

DIGITAL LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. ~~All~~ ~~questions~~ carry ~~equa~~l ~~marks~~. Part (a) of each question is compulsory. Attempt any* **two** *question from part (b), (c) & (d).*

Unit-I

1. (a) What do you mean by Universal Gate? 2

(b) Simplify the Boolean expression

$$f(A, B, C) = ABC + \bar{A}BC + A\bar{B}C + AB\bar{C} + \bar{A}B\bar{C}$$

and draw the logic diagram of simplified expression. 7

(c) State De-Morgan's theorem and prove it. 7

(d) A seven bit hamming code is received as 1000010. What was the code transmitted are what is the corrected code for even parity? 7

Unit-II

2. (a) What do you mean by standard SOP and POS? 2

(b) What do you mean by programmable logic devices? Write the comparison between PROM, PLA and PAL. 7

(c) Minimize the expression

$$f(A, B, C, D) = \sum m(0, 1, 8, 10, 13) + d(2, 5, 9)$$

using K-map and also implement using logic gate. 7

(d) Minimize the expression

$$f(A, B, C, D) = \sum m(1, 5, 6, 12, 13, 14) + d(2, 4)$$

using Quine-Mc Clusky method. 7

Unit-III

3. (a) How does a priority encoder differ from an ordinary encoder? 2

(b) Design and implement a SOP circuit that will generate an odd parity bit for a 4 bit input. 7

(c) Design 4-bit Binary to Gray code converter. 7

(d) Implement the following Boolean function using 8×1 multiplexer. 7

$$f(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 9) + d(10, 11, 12)$$

Unit-IV

4. (a) Is flip flop a sequential circuit, explain? 2

(b) Design a counter with the following binary sequence 0, 4, 2, 1, 6 and repeat. Use J-K flip-flop. 7

(c) Convert S-R to J-K flip-flop and J-K to D and T flip-flop. 7

(d) Draw and describe the working of parallel in series out (PISO) shift register. Explain how a number can be shifted in an out from such register. 7

Unit-V

5. (a) What is Propagation Delay? 2

(b) Draw and explain basic CMOS inverter circuit. 7

(c) Draw the circuit diagram and explain the operation of two input TTL NAND gate. 7

(d) Explain ECL digital logic family. 7